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Appl. No. 10/603,361  
Reply to Office Action of 5/17/2007  
Amdt. dated 08/09/2007

Attorney Docket No.: N1085-00089  
TSMC 2002-0917

**REMARKS/ARGUMENTS**

Claims 1-18 were pending in this application and each of claims 1-18 was rejected in the subject Office action. Claims 1, 14 and 17 are amended herein. Applicants respectfully request re-examination, reconsideration and allowance of each of pending claims 1-18.

I. **Rejections of Claims 1, 3-5, 9, 14-15, 17 and 18 under 35 U.S.C. § 103**

In the subject Office action, specifically in paragraph 2, claims 1, 3-5, 9 and 14-15, 17 and 18 were rejected under 35 U.S.C § 103(a) as being unpatentable over Clark et al. (U.S. Pat. No. 6,767,793), hereinafter "Clark" in view of Fried et al, (USPUB 2003/0113970), hereinafter "Fried". Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

Each of independent claims 1 and 17 recites the feature that the lower underlying device is a semiconductor fin with a planar top surface. As pointed out in Applicants' previous Response, each of independent claims 1 and 17 also recites the feature that the multiple gate electrode extends over and past both sides of the underlying semiconductor fin and that the multiple gate electrode has a planar upper surface formed only of the gate electrode material. Independent claims 1 and 17 have been amended and now each also recite that the top and the sides of the underlying semiconductor fin each form a portion of the channel of a single associated transistor. Support for this feature is found in the originally-filed specification, for example, on page 10, lines 4-6 which states "The channel (8), or channeled region, is a portion of the semiconductor fin (2) that is covered successively by the gate dielectric (10) and the

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gate electrode (3)". Figure 1 of the originally filed application therefore teaches that the channel region extends along the opposed sides and the top of the semiconductor fin.

Neither of the Clark or Fried references teach this feature.

In Clark, the gate electrode does not extend over the semiconductor fin. In Figure 31 relied upon by the Examiner, it can be seen that the gate electrodes 310 are only formed to the side of the SiGe layer 300. Thermal oxide 320 is exposed atop SiGe layer 300 and the gate electrode does not extend over top of the subjacent structure. The top portion of structure 300 of Clark therefore does not form a channel because there is no gate electrode disposed opposite the thermal oxide layer 320.

Fried, as illustrated in Figure 5B referred to by the Examiner, includes hard mask 14 atop fin 12. Hard mask 14 is NOT a gate dielectric and therefore Fried also does not teach the top of the fin being a transistor channel, much less a channel portion of a single transistor associated with channel portions on the top and opposed sides of the fin. In fact, Fried is distinctly directed to forming two transistors on opposed sides of the fin. Fried discusses, in paragraph [0007] "an asymmetric doped polysilicon gate where one side of the Fin (i.e., thin film semiconducting layer) includes an N<sup>+</sup> doped polysilicon gate and the other side of the Fin includes a P<sup>+</sup> doped polysilicon gate". Figure 5A of Fried illustrates N-type gate portion 24 on one side of fin 12 and P-type gate portion 26 on the other side of fin 12. There is no suggestion in Fried to utilize the top portion of the fin as a channel or portion of the channel because the gates formed on opposed sides of the fin are distinct. Indeed, the Fried disclosure is directed to the feature of an asymmetrical device with opposed N-type and P-type gates.

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Independent claims 1 and 17 are therefore distinguished from Clark in view of Fried and the rejection of claims 1, 3-5, 9, 14-15, 17 and 18 in this section should be withdrawn because claims 3-5, 9 and 14-15 depend from claim 1 and because claim 18 depends from claim 17. Applicants point out that dependent claim 14 has been  
5 amended to point out further distinguishing features of Applicants' invention.

**II. Rejection of Claims 2, 6-8 and 17**

In paragraph 4 of the subject Office action, claims 2, 6-8 and 17 were rejected under 35 U.S.C § 103(a) as being unpatentable over Clark in view of Fried as applied to claims 1 and 17, and further in view of Kinsbron. Applicants respectfully submit that  
10 these claim rejections are overcome for reasons set forth below.

As discussed in Applicants' previous Response, Kinsbron merely stands for the proposition that a photoresist layer has a planar top surface and will be of uniform thickness when applied over a planar surface. Kinsbron does not make up for the above-stated efficiencies of Clark in view of Fried and therefore independent claims 1  
15 and 17 as well as dependent claims 2, and 6-8, are distinguished from the references of Clark, Fried and Kinsbron.

The rejection of claims 2, 6-8 and 17 under 35 U.S.C § 103(a), should therefore be withdrawn.

**III. Rejection of Claims 10-13**

20 In paragraph 5 of the subject Office action, claims 10-13 were rejected under 35 U.S.C § 103(a) as being unpatentable over Clark in view of Fried as applied to claims 1 and 17, and further in view of Fried et al. (USP 6657252), hereinafter "Fried II".

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Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

As above, claim 1 is distinguished from Clark and Fried and claims 10-13 depend from claim 1. Fried II has apparently been relied upon for providing a gate dielectric material including silicon oxynitride, a high permittivity material and a thickness in the range of 3-100 angstroms but Fried II does not make up for the above-stated deficiencies of the combination of Clark and Fried. Because Fried II does not make up for these deficiencies, claim 1 and therefore dependent claims 10-13 are distinguished from the references of Clark, Fried and Fried II, taken alone or in combination.

The rejection of claims 10-13 under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Fried and further in view of Fried II, should therefore be withdrawn.

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**CONCLUSION**

Based on the foregoing, Applicants respectfully submit that each of claims 1-18 is in allowable form and the application is therefore in condition for allowance, which action is expeditiously and respectfully requested by Applicants.

The Assistant Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may associated with this communication, to Deposit Account 04-1679.

Respectfully submitted,

Dated: 09 August 2007

  
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